REMARKS

Some of the rejected claims have been amended. Support for the amendments can be found in the Application at, for example, p. 13, lines 2-3. No new matter has been added.

Applicant submits this Amendment "E" and Response for the Examiner's consideration. Reconsideration of the Application, as amended, in view of the following remarks is respectfully requested.

1. STATUS OF THE CLAIMS

Claims 1-10, 12-14, 16-20, 24-38, 40-44, 46, 50-52, and 54-58 were presented for examination and these claims stand rejected and pending in the application. Some of these claims are amended, the rejections are addressed below, and patentability of the claims over the cited reference is set forth below.

2. RESPONSE TO REJECTIONS

2.1. *Claim Rejections Under 35 U.S.C. § 103(a)*

The pending claims stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sadjadi, *et al.*, U.S. Pat. No. 5,883,436 (hereinafter "Sadjadi").

Sadjadi discloses a method "for forming a contact opening between two conductive features over a semiconductor substrate" wherein the discovery "is that oxide spacer technology can indeed be employed in conjunction with contact and via fabrication processes." Sadjadi, col. 2, *ll.* 27-29, col. 4, *ll.* 49-51.

Sadjadi generally refers in its disclosure to etch chemistries that have "a higher degree of selectivity to undoped oxide than to doped oxide." Sadjadi, col. 7, *ll.* 17-18, and *see also*, *e.g.*, Sadjadi, col. 5, *ll.* 32-34, 38-41.

Sadjadi, however, does not provide teachings concerning the etch processes that could

effectively be used, other than "[e]tch chemistries based on CHF_3, CF_4, N_2, and Ar combinations may be used, however the particular etch chemistry employed depends on the type of doping and dopant concentration in the dielectric films to be etched." Sadjadi, col. 5, *ll.* 38-41. In light of the novel character of etching with different selectivity to doped and undoped silicon dioxide, this teaching in Sadjadi appears more like an invitation to invent rather than as a disclosure to teach or suggest the presently claimed methods with all their limitations.

This lack of teachings is encountered in the context of a technological state of the art that Sadjadi itself characterizes as "hav[ing] focused development efforts into this technology under the notion that oxide spacer technologies cannot provide the etch selectivity necessary for the formation of suitably narrow contact openings." Sadjadi, col. 4, *ll.* 45-49. Sadjadi appears to characterize methodology that includes etching with different selectivity to doped and undoped silicon dioxide as being rather esoteric as compared with the conventional state of the art, and as implying peculiar features that the conventional state of the art had not taught or that, if previously addressed, had been treated under a notion that would actually teach away from the presently claimed methods.

Furthermore, as indicated in the Office Action, Sadjadi does not disclose or suggest any of the following elements and features in the claims:

(1) specifics on the use and type of plasma etcher;

(2) conductive plug formation in the context of the recited method steps;

(3) selective etching achieved with CH_2F_2 or CH_3F in the context of the recited method steps;

(4) materials and layering in gate formation;

(5) etching temperature conditions; and

(6) etching pressure conditions.

In addition, Sadjadi does not teach or suggest the use of an etching process with the

selectivity features that are presently recited, and Applicant has not been able to find in Sadjadi a teaching concerning the formation of gates on top of a SiO_2 pad layer. In addition to the foregoing features, Sadjadi does not teach other etch parameters recited in the claims, such as plasma density, plasma etch reactor cathode temperature, semiconductor material temperature, etching techniques, and chemical composition of the different structural elements of the semiconductor structure.

Sadjadi does not teach, suggest or provide any motivation to adopt the claimed methods with the limitations recited therein with an expectation that such methodology will effectively and successfully fulfill the goals of the invention.

The Office Action sets forth various official notices concerning some of the features that are neither taught nor suggested in Sadjadi. These official notices refer to the types of plasma etchers, the formation of a conductive plug in a SAC contact, the use of a plasma comprised of either CH_2F_2 or CH_3F, and the formation of gates on a wafer out of W polycide.

Applicant respectfully traverses these official notices. Official notice of facts beyond the record may be taken when such facts "are capable of such instant and unquestionable demonstration as to defy dispute" and provided that "the scope of any conclusions ... drawn [from any one of such notices]" is construed narrowly. *In re Ahlert*, 424 F.2d 1088, 1091 (C.C.P.A. 1970). Furthermore, official notices are not permitted in "areas of esoteric technology" and when the alleged "'knowledge' of the prior art ... might be peculiar to a particular art". *In re Ahlert*, 424 F.2d 1088, 1091 (C.C.P.A. 1970) (establishing that "[a]ssertions of technical facts in areas of esoteric technology must always be supported by citation to some reference work recognized as standard in the pertinent art and the appellant given, in the Patent Office, the opportunity to challenge the correctness of the assertion or the notoriety or repute of the cited reference" and that "[a]llegations concerning specific 'knowledge' of the prior art, which might be peculiar to a particular art should also be supported and the appellant similarly

given the opportunity to make a challenge." (Citations omitted)).

In light of the lack of teachings and suggestions in Sadjadi, including the lack of teachings and suggestions concerning the features indicated above, Applicant respectfully submits that (a) the items with respect to which an official notice is taken are not capable of instant and unquestionable demonstration as to defy dispute; (b) it has not been established, other than by the present Application, that the recited limitations, when taken from the items with respect to which official notice has been asserted, would successfully and effectively implement the claimed methods and would not be accompanied by the problems and detrimental consequences that afflict conventional techniques, such as those that rely on silicon nitride caps; and (c) application of the various official notices to the present claims would require a broad interpretation of conclusions drawn from such notices.

Furthermore, Sadjadi itself places the etching with different selectivity to doped and undoped silicon dioxide in a technological field that departs from the development focus that is conventional in the art, and that is contrary to the accepted notion in the art regarding the formation of contact openings. *See*, *e.g.*, Sadjadi, col. 4, *ll.* 45-49. This characterization tends to indicate that the present methodology is rather esoteric in the relevant technological context, and that the specific instances and features that play a role in its implementation are peculiar.

Even if, *arguendo*, the official notices taken in the Office Action were not traversable, Applicant respectfuly notes that "[i]n determining the differences between the prior art and the claims, the question under 35 U.S.C. [§] 103 is not whether the differences <u>themselves</u> would have been obvious, but whether the claimed invention <u>as a whole</u> would have been obvious." (Underlining in the original) (Citing *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 U.S.P.Q. 871 (Fed. Cir. 1983); *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 U.S.P.Q. 698 (Fed. Cir. 1983)). M.P.E.P. § 2141-02, p. 2100-118 (Aug. 2001). Therefore, focusing on differences in isolation may not lead to the establishment of a *prima facie* case of obviousness even if,

arguendo, the individual items with respect to which official notices are taken were known in the art.

In addition to the foregoing reasons, and even if, *arguendo*, the official notices taken in the Office Action were not traversable, the combination of the cited reference with the various official notices is improper because it fails to provide evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the reference with the various official notices. In this respect, it is well established that "[w]hen patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness" and " '[t]he factual inquiry whether to combine references must be thorough and searching.' It must be based on objective evidence of record. This precedent has been reinforced in myriad decisions, and cannot be dispensed with." (Citations and quotations omitted). *In re Lee*, ___ F.3d ___, (Fed. Cir. 2002), Federal Circuit docket number 00-1158 (vacating and remanding decision of the Board of Patent Appeals and Interferences that had rejected all of the claims as obvious). Applicant respectfully submits that the art of record fails to establish a sufficient teaching, motivation, or suggestion to select and combine the cited reference with the various official notices, even if, *arguendo*, the official notices taken in the Office Action were not traversable.

In taking the various official notices, the Office Action indicates that features in such official notices involve "alternative, and at least equivalent means for" accomplishing a certain objective. Applicant respectfully traverses this characterization, particularly in light of the how the ordinary skill in the art is described in Sadjadi. As noted above, Sadjadi states that "the semiconductor industry has focused development efforts into this technology under the notion that oxide spacer technologies cannot provide the etch selectivity necessary for the formation of suitably narrow contact openings." Sadjadi, col. 4, *ll*. 45-49. In light of the claim limitations that

are not taught or suggested by Sadjadi, and the state of the art as described by Sadjadi, Applicant respectfully submits that the limitations recited in the present claims are not merely alternative, and at least equivalent means for accomplishing the effective implementation of the claimed methods, but that they are part of an inventive effort as a whole for which the art of record provides not teaching, suggestion or motivation.

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation ... to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." Furthermore, the "teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (citations omitted) M.P.E.P. §§ 2142, 2143, p. 2100-121, -122 (8^{th} ed., Aug. 2001). For at least the reasons set forth above, Applicant respectfully submits that these criteria are not satisfied by the cited art.

Applicant notes the quote and cite to *In re Aller*, 220 F.2d 454 (C.C.P.A. 1955) provided in the Office Action. Applicant respectfully points out that this authority does not apply to the presently recited claims for at least the following reasons.

According to *In re Aller*, "[t]he process of appellants [was] identical with that of the prior art, except that appellants' claims specif[ied] lower temperatures and higher sulphuric acid concentrations than are shown in the reference." *In re Aller*, 220 F.2d 454, 45 (C.C.P.A. 1955). As shown hereinabove, the presently claimed methods are not identical with those disclosed in Sadjadi. Furthermore, the presently recited parameters may not be compared with those in Sadjadi's teachings because such reference is silent as to such parameters. Likewise, the items subject to the various official notices, even if, *arguendo*, such official notices were not traversable, do not provide any indication as to specific parameters for the claimed processes, so

that a comparison such as that relied on in *In re Aller* is not possible.

Applicant further submits that the use of the various recited parameters is not the result of mere optimization on the basis of known laws or patterns of behavior, but another manifestation of inventive work that is not taught or suggested by the art of record. This lack of teachings and the additional lack of teachings as indicated hereinabove with respect to Sadjadi and to the officially noticed items distinguish the conditions as set forth in *In re Aller* from those of the presently claimed processes.

Consequently, Applicant respectfully submits that the art of record does not support a *prima facie* case of obviousness regarding the present claims. Applicant respectfully requests the reconsideration and withdrawal of this rejection.

3. CONCLUSIONS

In view of the above, Applicant respectfully maintains that the present application is in condition for allowance. Reconsideration of the rejections is requested. Allowance of the pending claims at an early date is solicited.

In the event that the Examiner finds any remaining impediment to a prompt allowance of this application which could be clarified by a telephonic interview, or which is susceptible to being overcome by means of an Examiner's Amendment, the Examiner is respectfully requested to initiate the same with the undersigned attorney.

Dated this 18th day of June 2002.

Respectfully submitted,

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Marked up Version of the Pending Claims Under 37 C.F.R. § 1.121(c)(1)(ii):

Please amend the claims as follows and in accordance with 37 C.F.R. § 1.121(c)(1)(ii), by which Applicant submits the following marked up version only for the claim being changed by the current amendment, wherein the markings are shown by brackets (for deleted matter) and/or underlining (for added matter):

1. (Thrice Amended) A process for forming a contact opening to a semiconductor material, said process comprising:

forming an undoped silicon dioxide layer over a layer of semiconductor material;

selecting an etch process that is selective to undoped silicon dioxide, silicon, and silicon nitride;

forming a doped silicon dioxide layer over said undoped silicon dioxide layer; and

selectively removing by said etch[ing] process at a total etch pressure in the range from about 1 millitorr to about 400 millitorr and by using an etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, CH_3F, and combinations thereof, a portion of said doped silicon dioxide layer at a material removal rate that is higher for doped silicon dioxide than for undoped silicon dioxide or for said layer of semiconductor material to form an opening extending to a contact surface on said layer of semiconductor material.

5. (Twice Amended) A process as recited in Claim 4, wherein said plasma etching process has a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3.

13. (Four Times Amended) A process for forming contact to a semiconductor material, said process comprising:

forming an undoped silicon dioxide layer over a layer of monocrystalline silicon;

forming a doped silicon dioxide layer over said undoped silicon dioxide layer, said doped silicon dioxide layer being selected from the group consisting of BPSG, PSG, and BSG;

forming a layer of photoresist over said doped silicon dioxide layer;

patterning said layer of photoresist;

<u>selecting an etch process that is selective to undoped silicon dioxide, silicon, and silicon nitride;</u>

etching <u>with said etch process</u> said doped silicon dioxide layer through the pattern of said layer of photoresist at a material removal rate that is higher for doped silicon dioxide layer than for undoped silicon dioxide layer or for said layer of monocrystalline silicon to form an opening extending to said layer of monocrystalline silicon, said etching being a plasma etching process in a plasma etcher, said plasma etching process being conducted:

at a pressure range from about 1 millitorr to about 400 millitorr;

a temperature range of the cathode that is from about 10°C to about 80°C;

in a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3 with a fluorinated chemical etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, CH_3F, and combinations thereof.

18. (Thrice Amended) A process for forming a contact to a semiconductor substrate comprising:

providing a gate oxide layer over the semiconductor substrate;

providing a pair of gate stacks in spaced relation to one another on the semiconductor substrate, each of said gate stacks having at least one conductive layer formed therein and an undoped silicon dioxide layer extending over said conductive layer;

forming a spacer, composed of undoped silicon dioxide, adjacent to each of said gate stacks;

forming a doped silicon dioxide layer over said pair of gate stacks and over said exposed surface on said semiconductor substrate;

selecting an etch process that is selective to undoped silicon dioxide, silicon, and silicon nitride;

selectively removing with said etch process a portion of said doped silicon dioxide layer between said pair of gate stacks to expose said surface on said semiconductor substrate, while removing less of said undoped silicon dioxide layer over said pair of gate stacks, wherein said etching removes doped silicon dioxide at a material removal rate that is at least 10 times higher than for each of undoped silicon dioxide, the spacer, and the semiconductor substrate.

29. (Twice Amended) A process as recited in Claim 18, wherein selectively removing said doped silicon dioxide layer comprises:

forming a layer of photoresist over said doped silicon dioxide layer;

selecting an etch process that is selective to undoped silicon dioxide, silicon, and silicon nitride;

patterning said layer of photoresist; and

etching with said etch process said doped silicon dioxide layer through the pattern of said layer of photoresist in a plasma etching process in a plasma etcher, said plasma etching process being conducted:

at a pressure range from about 1 millitorr to about 400 millitorr;

a temperature range of reactor cathode that is from about 10°C to about 80°C;

a temperature range of the semiconductor material is from about 40°C to about 130°C;

in a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3; and

with a fluorinated chemical etchant.

31. (Four Times Amended) A process for forming a contact to a semiconductor material comprising:

depositing a gate oxide layer over a layer of silicon of a semiconductor substrate;

depositing a polysilicon layer over said gate oxide layer;

depositing a refractory metal silicide layer over said polysilicon layer;

depositing an undoped silicon dioxide layer over said refractory metal silicide layer;

selectively removing portions of said undoped silicon dioxide layer, said refractory metal silicide layer, said polysilicon layer, and said gate oxide layer so as to form a pair of gate stacks separated by an exposed portion of said silicon layer, each said gate stack having a lateral side perpendicular to said gate oxide layer and being comprised of:

said undoped silicon dioxide layer as the top layer thereof;

said refractory metal silicide layer;

said polysilicon layer; and

said gate oxide layer as the bottom layer thereof;

forming a spacer on the lateral side of each said gate stack from a layer of spacer material;

<u>selecting an etch process that is selective to undoped silicon dioxide, silicon, and silicon nitride;</u>

depositing a doped silicon dioxide layer over said pair of gate stacks and over said exposed portion of said silicon layer, said doped silicon dioxide layer being is selected from the group consisting of BPSG, PSG, and BSG; and

etching <u>with said etch process</u> said doped silicon dioxide layer with a plasma etching system having a plasma density in a range from about 10^9 ions/cm^3 to about

10^{13} ions/cm^3 in an etcher selected from the group consisting of RF RIE, MERIE plasma etching system, and high density plasma etching system, said plasma etching system having a pressure range from about 1 millitorr to about 400 millitorr, said doped silicon dioxide layer being etched between said pair of gate stacks so as to expose said exposed portion of said silicon layer, said etching having a material removal rate that is higher for doped silicon dioxide than for undoped silicon dioxide, said spacer material, or silicon, said etching of said doped silicon dioxide being conducted with a fluorinated chemical etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, CH_3F, and combinations thereof.

37. (Four Times Amended) A process for forming a gate structure comprising:

providing a multilayer structure comprising a layer of silicon dioxide over a layer of silicon;

depositing a layer of undoped silicon dioxide over said multilayer structure using a precursor having a gaseous silane, hydrogen, and oxygen flow;

forming a first layer of photoresist over said layer of undoped silicon dioxide;

patterning said first photoresist layer to form a first pattern;

etching said layer of undoped silicon dioxide and said multilayer structure through said first pattern to expose a contact surface on at least a portion of said layer of silicon;

depositing a layer of a nonconductive material over said layer of undoped silicon dioxide and said contact surface on said layer of silicon;

etching said layer of said nonconductive material to thereby create a spacer over a lateral side of said layer of undoped silicon dioxide and over a lateral side of said multilayer structure, said spacer being generally perpendicular to said layer of silicon;

removing said first layer of photoresist;

depositing a doped silicon dioxide layer over said multilayer structure;

forming a said second layer of photoresist over said layer of doped silicon dioxide;

patterning said second layer of photoresist to form a second pattern;

<u>selecting an etch process that is selective to undoped silicon dioxide, silicon, and silicon nitride;</u>

etching <u>with said etch process</u> said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch that is an anisotropic plasma etch using fluorinated chemical etchants selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, CH_3F, and combinations thereof, and that etches through said

second pattern to expose said contact surface on said layer of silicon, said etching having a material removal rate that is at least 10 times greater for doped silicon dioxide than for undoped silicon dioxide, photoresist, or nonconductive material;

removing said second layer of photoresist; and

forming a contact plug composed of a conductive material in contact with said contact surface on said layer of silicon.

44. (Four Times Amended) A process for forming a gate structure comprising:

providing a multilayer structure situated over a layer of silicon and comprising layers of gate oxide, polysilicon, and refractory metal silicide;

depositing a layer of undoped silicon dioxide over said multilayer structure using a precursor having a gaseous silane, hydrogen, and oxygen flow;

forming a first layer of photoresist over said layer of undoped silicon dioxide;

patterning said first photoresist layer to form a first pattern;

etching said layer of undoped silicon dioxide and said multilayer structure through said first pattern to expose a contact surface on at least a portion of said layer of silicon;

removing said first layer of photoresist;

depositing a layer of a nonconductive material over said layer of undoped silicon dioxide and said contact surface on said layer of silicon;

etching said layer of said nonconductive material to thereby create a spacer over a lateral side of said layer of undoped silicon dioxide and over a lateral side of said multilayer structure, said spacer being generally perpendicular to said layer of silicon;

depositing a doped silicon dioxide layer over said multilayer structure and over said contact surface on said layer of silicon, wherein said doped silicon dioxide layer is selected from the group consisting of BPSG, PSG, and BSG;

forming a second layer of photoresist over said layer of doped silicon dioxide;

patterning said second layer of photoresist to form a second pattern;

<u>selecting an etch process that is selective to undoped silicon dioxide, silicon, and silicon nitride;</u>

etching <u>with said etch process</u> said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch through said second pattern to expose said

contact surface on said layer of silicon, said etching having a material removal rate that is at least 10 times greater for doped silicon dioxide than for undoped silicon dioxide, photoresist, or nonconductive material, wherein said carbon fluorine etch is an anisotropic plasma etch using a fluorinated chemical etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, CH_3F, and combinations thereof, wherein said etching of said doped silicon dioxide utilizes a plasma etching system having a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3 at a pressure in a range from about 1 millitorr to about 400 millitorr, the temperature range of said reactor cathode during said plasma etch being about 10°C to about 80°C, and the temperature range of the semiconductor material during said plasma etch being in the range of about 40°C to about 130°C;

removing said second layer of photoresist; and

forming a contact plug comprising a conductive material in contact with said contact surface on said layer of silicon.

50. (Four Times Amended) A method of forming a self-aligned contact, said method comprising:

providing a pair of gate stacks in spaced apart relation to one another on said semiconductor substrate, each of said gate stacks being covered by an undoped silicon dioxide layer;

forming a spacer adjacent to each of said gate stacks;

forming a doped silicon dioxide layer over said pair of gate stacks and over said semiconductor substrate;

forming a layer of photoresist over said silicon dioxide layer;

<u>selecting an etch process that is selective to undoped silicon dioxide, silicon, and silicon nitride;</u>

patterning said layer of photoresist; and

selectively removing <u>with said etch process</u> a portion of said doped silicon dioxide layer between said pair of gate stacks using an etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, CH_3F, and combinations thereof, to expose a contact surface on said semiconductor substrate through said pattern of said layer of photoresist, while removing less of said undoped silicon dioxide layer over said pair of gate stacks than doped silicon photoresist, said undoped silicon layer being capable of resisting said selective removal process thereby causing said selective removal process to be self-aligning between said pair of gate stacks.

58. (Once Amended) A process for forming a contact opening to a semiconductor material, said process comprising:

forming an undoped silicon dioxide layer over a layer of semiconductor material;

selecting an etch process that is selective to undoped silicon dioxide, silicon, and silicon nitride;

forming a BSG layer over said undoped silicon dioxide layer; and

selectively removing by said etch[ing] process at a total etch pressure in the range from about 1 millitorr to about 400 millitorr and by using an etchant selected from the group consisting of C_2F_6, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, CH_3F, and combinations thereof, a portion of said doped silicon dioxide layer at a material removal rate that is higher for doped silicon dioxide than for undoped silicon dioxide or for said layer of semiconductor material to form an opening extending to a contact surface on said layer of semiconductor material.

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